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# Adaptive Virtual Impedance Scheme for Selective Compensation of Voltage Unbalance and Harmonics in Microgrids

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***Abstract*— This paper presents a two-level hierarchical control approach for voltage source inverters used to interface Distributed Generators (DGs) in microgrid applications. The control structure comprises primary and secondary levels. The primary level is a local controller, which consists of voltage and current inner control loops in order to fix the filter capacitor voltage and a virtual impedance loop mainly for voltage harmonics and unbalance compensation. The virtual impedance is set by the central secondary controller to mitigate the voltage distortion at sensitive load bus (SLB). Secondary controller is connected to a measurement unit to obtain the data of voltage harmonics and unbalance at microgrid SLB and broadcasts the commands for adjusting the virtual impedance of each unit. A general case with a combined voltage harmonic and unbalance distortion is considered. In such a case, voltage distortion is mitigated by selective insertion of capacitive virtual impedances for negative sequence of fundamental component as well as positive and negative sequences of main harmonics. The values of virtual capacitances are determined based on the required voltage quality at the load bus; thus, this scheme is titled as adaptive virtual impedance. Experimental results are presented to demonstrate the effectiveness of the proposed control approach.**

***Index Terms*— Distributed generator (DG), harmonics, microgrid, unbalance, virtual impedance.**

## I. INTRODUCTION

Distributed Generators (DGs) are often connected to the electrical systems through a power-electronic interface converter. A cluster of DGs and loads can form a local grid, called *Microgrid*, which is able to operate in grid-connected and islanded modes [1]. Islanded microgrids are discussed in IEEE Std. 1547.4-2011 [2] and will be studied in the present paper. In ac microgrids, the last stage of DGs interface converter is an inverter, which in islanded operation is often controlled to regulate output voltage and frequency [3]. However, recently some control approaches are proposed to control the inverter for compensation of power quality problems [4]-[10].

The scheme of [4] is based on a two-inverter (shunt-series) interface converter to control power flow and to compensate the voltage unbalance. This structure can be unattractive due to high cost and volume of the interface converter. In [5], each DG unit of microgrid is controlled as a negative sequence conductance to compensate voltage unbalance. An autonomous voltage unbalance compensation scheme which works based on the local measurements is proposed in [6] for DG units of an islanded microgrid. In [7] and [8], the inverters emulate a resistance at harmonic frequencies to compensate voltage harmonic distortion. The methods presented in [5]-[8] are designed for compensation of voltage unbalance or harmonics at each DG terminal while usually it is preferred to have a good power quality at "Sensitive Load Bus (SLB)" of the microgrid. Based on this, a hierarchical structure is presented in [9] to enhance voltage quality at SLB.

As explained in [10], another idea for compensation of power quality problems is to apply capacitive virtual impedances. The capacitive impedance presented in [10] has a fixed value and is realized by a negative inductance equal to the output inductor of LCL filter of interface inverters. This way, the voltage quality after the LCL filter is improved, noticeably. Moreover, the control structure is much simpler than hierarchical scheme of [9]. However, the quality of SLB voltage is not controlled in [10] and it can be a problem, if SLB is electrically far from the LCL filter output. In addition, it is assumed in [10] that all inverters are terminated to LCL filters. This assumption cannot be generalized to all applications.

In this paper, the concept of secondary control is applied to adaptively set the value of virtual impedance (capacitance). To consider a general case, a nonlinear load with one-phase disconnection is connected to the microgrid to generate fundamental voltage unbalance as well as negative and positive sequences of harmonics. In the proposed scheme, secondary controller determines the virtual capacitances which should be inserted for negative sequence of fundamental component and for main harmonic orders (here $3^{rd}$, $5^{th}$ and $7^{th}$ harmonics) in a

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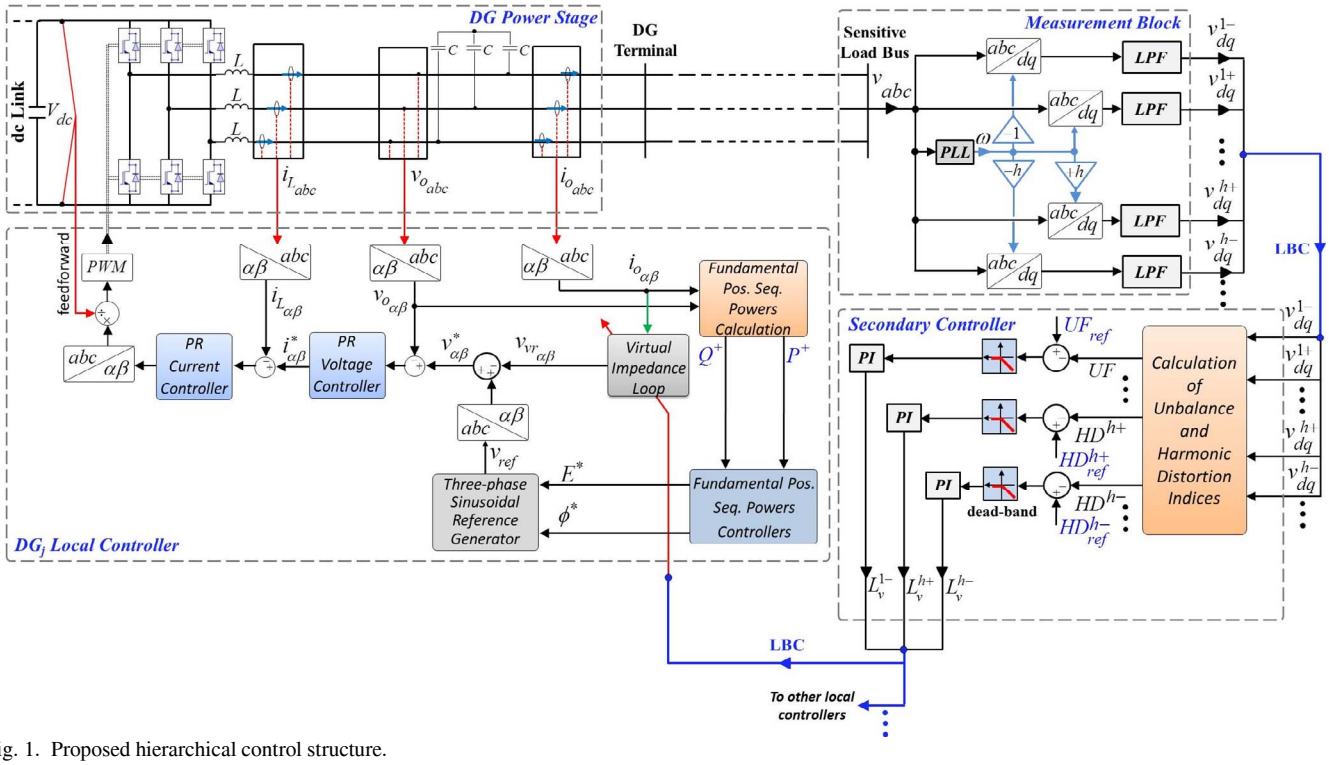



Fig. 1. Proposed hierarchical control structure.

selective way. Note that in the case of unbalanced loading, triplen harmonics will also have positive and negative sequences [9]. The control objective is to reduce SLB voltage distortion to the desired level.

## II. Proposed Control Structure

The structure of the voltage source inverter (VSI) and the two-level control scheme is depicted in Fig. 1. VSI consists of a three phase PWM inverter (output stage of DG interface) and an LC (or LCL) filter. Primary level encompasses microgrid DGs local controllers which mainly consist of proportional-resonant (PR) voltage and current controllers, power droop controllers, and virtual impedance loop. The control system is designed in stationary ($\alpha\beta$) reference frame. Thus, Clarke equations are applied to transform the voltages and currents between *abc* and $\alpha\beta$ frames. As it can be seen in Fig. 1, the reference of the DG capacitor voltage ($v^*_{\alpha\beta}$) is formed by power droop controllers and selective virtual impedance loop. Then, the reference current ($i^*_{\alpha\beta}$) is generated based on the instantaneous capacitor voltage in $\alpha\beta$ frame ($v_{o_{\alpha\beta}}$) and $v^*_{\alpha\beta}$. Furthermore, LC filter inductor current is transformed to $\alpha\beta$ frame ($i_{L_{\alpha\beta}}$) and controlled by the current controller to generate the reference voltage for the PWM block. In addition, a feedforward loop is included in order to take the small variations of dc link voltage ($V_{dc}$) into account. Details about droop controllers and voltage/current loops can be found in [9] and [11].

As it can be seen in Fig. 1, the central secondary level is implemented by using some PI controllers that broadcast the reference values to each DG for compensation of voltage unbalance and harmonic distortion to the required level. The secondary controller can be far from DGs and SLB. Thus, SLB voltage information is sent to this controller by means of low bandwidth communication (LBC). Low bandwidth is preferred since the control performance will not be dependent on the availability of a high bandwidth communication. To make sure that LBC is sufficient, positive and negative sequences of SLB voltage fundamental and main harmonic components are extracted in *dq* frame. This way, the resultant values are dc and can be transmitted by means of LBC. In Fig. 1, superscripts "+", "–", "1" and "*h*" represent positive sequence, negative sequence, fundamental component and $h^{\text{th}}$ harmonic component, respectively. More explanations about measurement block are provided in [9].

The structure of the secondary controller and virtual impedance loops are explained in the following subsections.

### A. Secondary Controller

The details of the secondary controller are also depicted in Fig. 1. As seen, *dq* components of SLB voltage fundamental positive and negative sequences ($v^{1+}_{dq}$ and $v^{1-}_{dq}$) and $h^{\text{th}}$ harmonic positive and negative sequences ($v^{h+}_{dq}$ and $v^{h-}_{dq}$) are used to calculate voltage unbalance factor ($UF$) and $h^{\text{th}}$ harmonic distortion indices ($HD^{h+}$ and $HD^{h-}$). For this, the following equations can be applied:

$$\%UF = \frac{\sqrt{\left(v_d^{1-}\right)^2 + \left(v_q^{1-}\right)^2}}{\sqrt{\left(v_d^{1+}\right)^2 + \left(v_q^{1+}\right)^2}} \times 100 \quad (1)$$

$$\%HD^{h\pm} = \frac{\sqrt{\left(v_d^{h\pm}\right)^2 + \left(v_q^{h\pm}\right)^2}}{\sqrt{\left(v_d^{1+}\right)^2 + \left(v_q^{1+}\right)^2}} \times 100 \quad (2)$$

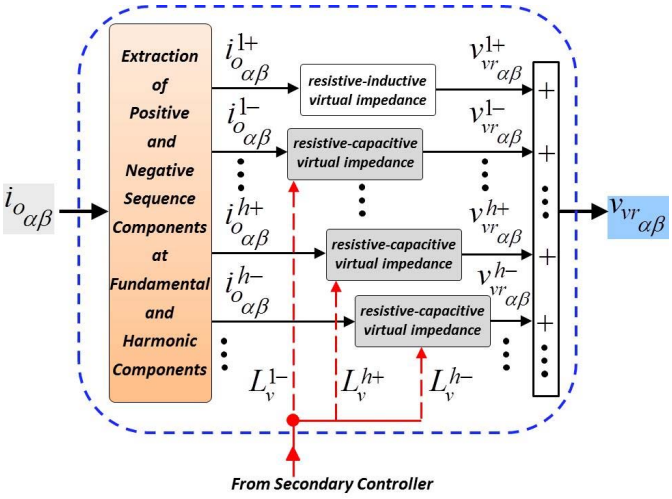



Fig. 2. Proposed adaptive virtual impedance scheme.

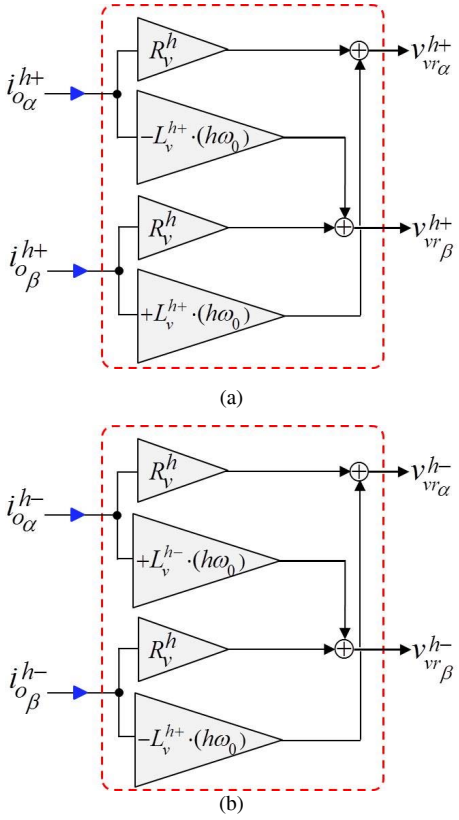



Fig. 3. Details of resistive-capacitive virtual impedance for $h^{th}$ harmonic. (a) positive sequence, (b) negative sequence

Then, $UF$, $HD^{h+}$ and $HD^{h-}$ are compared with the reference values ($UF_{ref}$, $HD^{h+}_{ref}$ and $HD^{h-}_{ref}$, respectively) and the errors are fed to proportional-integral (PI) controllers. The outputs of these controllers are reference values for negative inductances ($L_v^{1-}$, $L_v^{h+}$ and $L_v^{h-}$), which act as capacitances to compensate voltage distortion of SLB. Finally, these references are sent to each inverter local controller (primary level). Note that if $UF$, $HD^{h+}$ or $HD^{h-}$ are less than the reference values, the respective dead-band block shown in Fig. 1 prevents the increase of the distortion by the PI controller.

### *B. Adaptive Virtual Impedance Scheme*

The general structure of the proposed adaptive virtual block is illustrated in Fig. 2. It consists of resistive-inductive structure for fundamental positive sequence component and resistive-capacitive scheme for other current components. As it can be observed, the inverter output current in stationary frame ($i_{o\alpha\beta}$) is fed to the virtual impedance block and then, its components are extracted. Afterwards, each component is applied to the respective sub-block. Finally, the outputs of these sub-blocks are added together and inserted as a reference for voltage controller, as shown in Fig. 1.

The resistive-inductive sub-block of Fig. 2 is to enhance the performance of droop controllers and to make the system more damped [6], [11]. The resistive part of resistive-capacitive sub-blocks can be included to improve the sharing of fundamental negative sequence and harmonic components of load current among inverters. The performance of these virtual resistances is investigated in the previous works (e.g. [9] and [10]) and will not be discussed in the present paper. As mentioned before, the capacitive parts of the virtual impedance block are adaptively set by the secondary controller.

The way of creating a resistive-capacitive virtual impedance in $\alpha\beta$ frame for positive and negative sequences of $h^{th}$ harmonic is depicted in Fig. 3. In this figure, $R_v^h$ is the virtual resistance for sharing $h^{th}$ current harmonic among inverters and $\omega_0$ represents the system fundamental angular frequency. Note that usually same virtual resistances are applied for both sequences of harmonics [9]. The scheme of Fig. 3(b) can be applied for negative sequence of fundamental component by replacing $h$ by 1. More descriptions can be found in [10].

## III. Experimental Results

Fig. 4 shows the general scheme and the photo of experimental setup. The test system represents a two-DG islanded microgrid. As it can be seen in Fig. 4(a), a diode rectifier is connected to SLB as the nonlinear load. In order to create unbalanced voltage distortion, it is assumed that one phase of this load is disconnected. Note that no further load is connected to SLB to have the experimental setup as simple as possible. However, in practice, the distortion created by the nonlinear load can cause malfunction of the sensitive loads connected to the same bus or a bus in electrical proximity. Switching frequency of the DGs inverters is 10 kHz. Inverters switching is controlled by a DS1103 dSPACE card. "*dSPACE Control Desk*" is used as the user interface. The test system

parameters are listed in Table I. The details of designing primary and secondary controllers have been provided in [9] and [11].

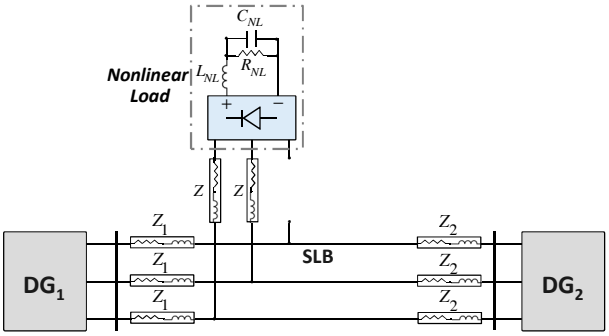
It should be stated that since the effect of resistive virtual impedances at harmonic frequencies on sharing of current harmonics among inverters are previously shown in [9] and [10], these resistances are not considered in the experiment and only the compensation of voltage distortion by capacitive virtual impedances is studied. However, basic resistive-inductive structure of virtual impedance for fundamental positive-sequence component is included.

Secondary controller is activated at t=3s. This control level consists of PI controllers for fundamental negative sequence and positive and negative sequences of third, fifth and seventh harmonics. The reference values of secondary control for unbalance and harmonic distortions are $UF_{ref} = 0.2\%$ and $HD_{ref}^{3\pm} = HD_{ref}^{5\pm} = HD_{ref}^{7\pm} = 0.5\%$. Fig. 5 shows the values of negative inductances $L_v^{1-}$ and $L_v^{3\pm}$ which are determined by secondary controller. A similar behavior was observed for $L_v^{5\pm}$ and $L_v^{7\pm}$, but not included to avoid paper over-length.

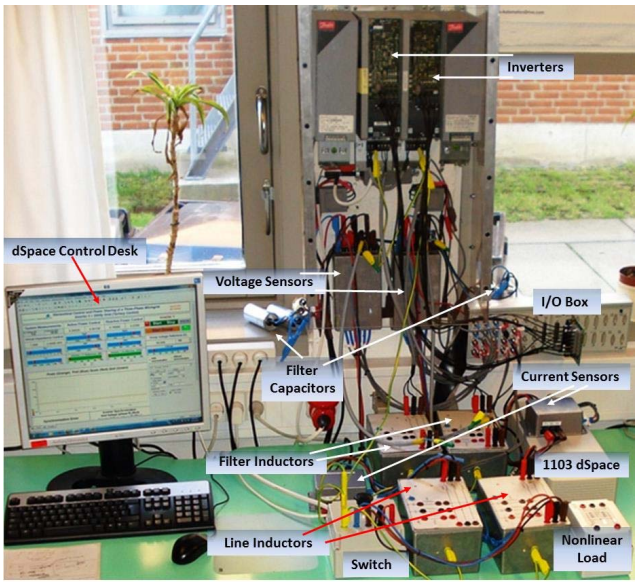
Before secondary control activation, the DGs output voltages (at LC filter capacitance terminal) is distortion-free; but, after insertion of negative inductances, these voltages become distorted as explained in [10] to improve SLB voltage quality. For instance, the variations of $UF$, $HD^{3+}$ and $HD^{5-}$ at DGs terminal and SLB are depicted in Fig. 6. To better observe the voltage quality improvement at SLB, Fig. 7 shows the three-phase voltage waveform of SLB, before and after secondary control activation. It is worth noting that due to the experimental limitations, it was not possible to create more voltage distortion at SLB to appreciate the compensation effectiveness more clearly; however, the authors think that the presented results are sufficient to demonstrate the performance of the proposed scheme.

TABLE I
POWER STAGE PARAMETERS

| dc link voltage | LC Filter Inductance | LC Filter Capacitance |
|---|---|---|
| $V_{dc}$ (V) | $L$ (mH) | $C$ (μF) |
| 650 | 1.8 | 25 |
| Distribution Lines | Nonlinear Loads | Nonlinear Load Tie Line |
| $Z_1/Z_2$ (Ω,mH) | $C_{NL}/R_{NL}/L_{NL}$ (μF)/(Ω)/(mH) | $Z$ (Ω,mH) |
| 0.3,5.4/0.2,3.6 | 235/200/0.084 | 0.1, 1.8 |

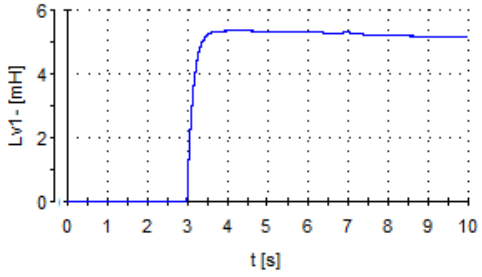



(a)

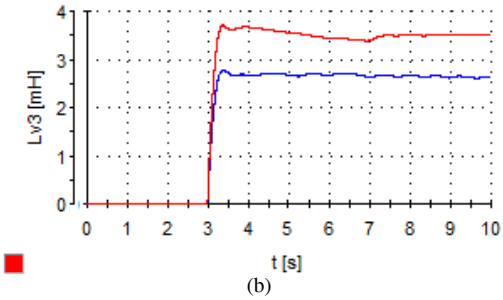



(b)

Fig. 4. Test system: (a) general scheme, (b) photo of experimental setup.




(a)




(b)

Fig. 5. Reference inductance values generated by secondary controller. (a) fundamental negative sequence, (b) third harmonic positive (red) and negative (blue) sequences.

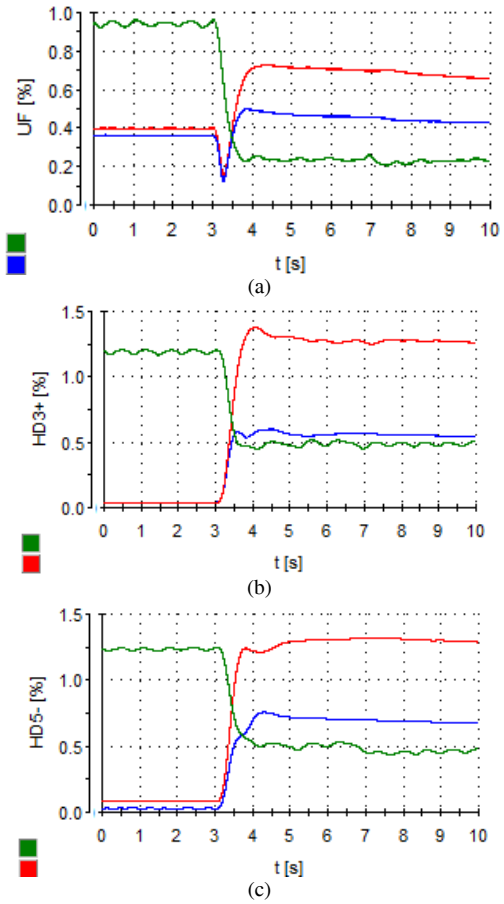



Fig. 6. Variations of voltage distortion indices: (a) unbalance factor, (b) positive sequence of 3rd harmonic, (c) negative sequence of 5th harmonic (blue: $DG_1$, red: $DG_2$, green: SLB).

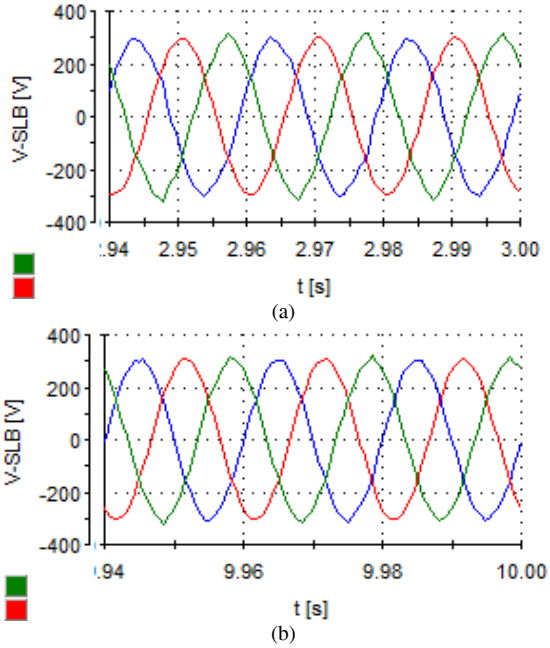



Fig. 7. SLB voltage waveforms: (a) before compensation, (b) after compensation.

## IV. Conclusions

An adaptive capacitive virtual scheme has been proposed based on a hierarchical control structure. The control objective is to mitigate the voltage quality problems at sensitive load bus of a microgrid to the desired level. The values of capacitive virtual impedances for fundamental negative sequence component and positive and negative components of selected harmonics are determined by a central secondary controller and then sent to the DGs local controllers. It was shown by the experimental results that addition of virtual capacitances distorts the output voltage of DGs to ensure a high quality of voltage at SLB.

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