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Polyphase Boost Converter with Digital Control

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Keywords; Digital control, Boost converter, Current control mode, Parallel operation, Polyphase, Unity power factor

Abstract

Boost d.c.-d.c. converters have very good source interface properties. The input inductor makes the source current smooth and hence these converters provide very good EMI performance. On account of this good property, the boost converter is also the preferred converter for off-line UPF rectifiers. One of the issues of concern in these converters is the large size of the storage capacitor on the dc link. The boost converter suffers from the disadvantage of discontinuous current injected to the load. The size of the capacitor is large. Further, the ripple current in the capacitor is as much as the load current; hence the ESR specification of the tank capacitor is demanding. This paper presents the polyphase boost converter, which overcomes the problem of high ripple current in the tank capacitor, which has not been discussed earlier. Comparison between the specifications of single stage and multistage is thoroughly examined. Digital control is more convenient for such a topology on account of the requirement of synchronization, phase shifted operation and current balancing. The control method is simpler and faster than its original form [10]. It does not depend on the previous duty ratio and it has been tested on four boost converters in parallel. Each is a 35W unit switched at 200 kHz. Experimental results in digital control, synchronization operation and current sharing are presented. The control method is implemented using a TI's general purpose Digital Signal Processor eZdspF2812. This control scheme is applicable for PFC rectifiers as well.

Introduction

In designing d.c.-d.c. converters, parameters such as ratio of energy stored in inductor and capacitor to energy delivered to load in one period, maximum current in the switch and the value of the RMS current in the output capacitor have great importance and it is necessary to be considered.

The motivation for this work is expressed through consideration of the above parameters in per unit measures for the two basic converters namely the buck and the boost converter [1]. Consider the boost converter in Fig.1 with per unit values defined as

$V_{dc} = 1$, $D = 0.5$, $T_s = F_s = 1$, $E_o = 1$, $P_o = 1$, $\Delta I_L/I_L = 20$ %,

$\Delta V_o/V_o = 1$ %

Table I gives the reactive elements and their energy storage capacity for the basic converters. From the table it is obvious that the boost converter requires total energy storage far in excess of buck converter.

One way to reduce the storage requirement is increasing the switching frequency of the converter. However, this is not feasible in all instances. During the on state of the switch, the capacitor has to supply the entire load current in the boost converter. This discontinuity of current in the capacitor increases the RMS value of current and also increases the amount of capacitance, which is needed to keep the ripple voltage low. The power dissipation in the ESR of the capacitor is high. This is specially so in the emerging application areas of automotive power conversion, where the input voltage is low (typically 12V) and large voltage boost (4 to 5) are desired. In the UPF rectifier applications, the input voltage varies from zero to maximum value twice in every cycle of the a.c. input voltage. The duty cycle therefore varies in the full range of zero to one. The inductor current varies from zero to nominal current twice in every a.c. cycle of the input current. On account of the wide operating point variation, the design of the power circuit as well as the closed loop controller is a demanding task. In standard designs it is not uncommon to see tank capacitors one or two orders of magnitude higher than the ideally required capacitance A way to overcome this problem is using polyphase operation with appropriate phase shift in the control circuit of main switches [2,3]. Fig 2 shows such a polyphase boost converter ($N = 4$). Fig. 3 shows the conduction intervals of the four switches in the converter. At any time at least one of the converters is supplying the load in addition to the capacitor. The frequency of ripple current in the output capacitor is N times compared to the single stage and therefore the value of the capacitor required can be reduced. The same circuit topology is also applicable to UPF rectifiers. Fig. 4 shows such a power circuit.

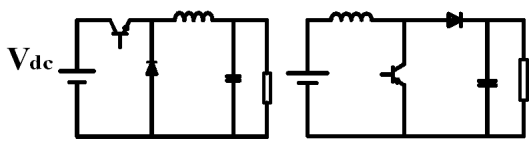

Fig. 1: Buck & Boost Converter respectively

Table: Comparing Buck & Boost Converters in terms of per unit values for the same output power

	L (per unit)	C (per unit)	V_o (per unit)	E_t/P_oT_s	E_e/P_oT_s
Boost Converter	2.5	12.5	2	1.25	25
Buck Converter	1.25	10	0.5	1.25	1.25

In such a scheme, the following advantages are observed.

– output capacitor is rated for lower ripple current and higher ripple frequency (N*Fs);
– source current has higher ripple and at higher frequency (N*Fs);
– the polyphase converter may be operated with less number of stages when the load current is low; this will lead to operation under CCM at light load and better efficiency.

The control of polyphase converters has to possess several features such as:

– high speed of switching (typically 100 kHz);
– synchronization (typically up to 16 converters);
– current control (for better protection);
– selective topology masking (for variable load operation).

Digital control has the features of programmability, modularity and better dynamic response. Nowadays they have become more popular because of the decreasing cost of hardware such as microprocessors, analog to digital converters and digital to analog converters [9]. Power supplies that switch at very high frequencies are now feasible due to the recent advances in the area of high speed digital circuits. Until recently lot of efforts have been done in developing digital current control [8-11]. The direct method of digital current control in [11] requires a large amount of I_{ref} in terms of per unit value in coding the digital implementation. The method proposed in the paper is based on [10] with a modification in the control rule, which has been computed based on a single cycle. It is simpler, faster and has been validated in experiment.

This paper discusses first basic operation of polyphase boost converter in analog and digital control. Digital current control law and application to polyphase boost converter is then performed. After that, comparison between the specifications of a single and polyphase boost converter is performed. The following section explains the realization of the circuit. Experimental results and conclusions close the paper.

Polyphase operation

Fig. 5 shows the basic schematic and control operation of a polyphase boost converter. Each stage has an independent current mode control loop, which uses the same reference current. The reference current in turn is generated by the outer voltage control loop. For correct operation of polyphase boost converter each PWM gate signal is required to have 90 degrees phase shift with respect to the previous one. To generate these PWM signals a synchronization circuit is needed. The controller realized with analog blocks is shown in Fig. 5. Though practicable, the analog realization has certain limitations. The number of converters in parallel, their synchronization angles, etc has to be decided in advance for any application. Control over the choice of switching frequency is not total. Because of these disadvantages in the analog implementation of the control an alternate digital realization of the polyphase controller is presented. The need for a different implementation is thus completely understood.

Fig. 6 shows the architecture of digital control, which has been used here for the polyphase boost converter. A PI controller based on the error signal from the outer voltage loop builds the reference current. The inductor current in each of the converters or a representative sample of the inductor currents is compared with current reference. Accordingly the individual duty ratios or a single common duty ratio is imposed on the switches.

In digital implementation modularity of the system is preserved. Adding extra stages or changing the switching frequency needs only a modification in software.

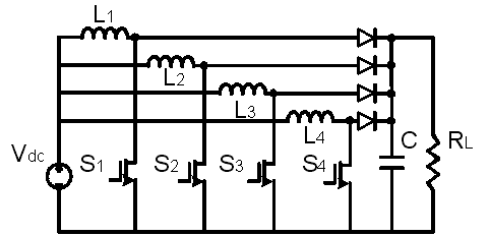

Fig. 2: Polyphase Boost Converter

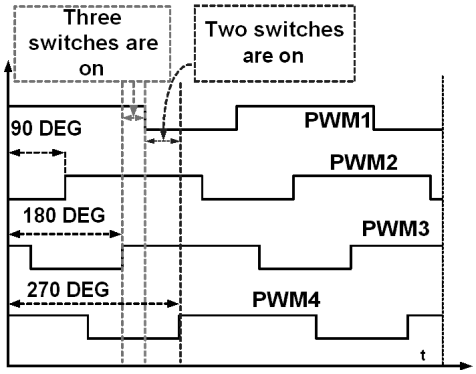

Fig. 3: Phase shifted PWM Waveforms

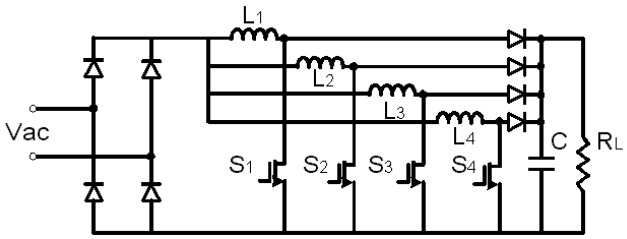

Fig. 4: Unity Power Factor Rectifier with Polyphase Boost Converters

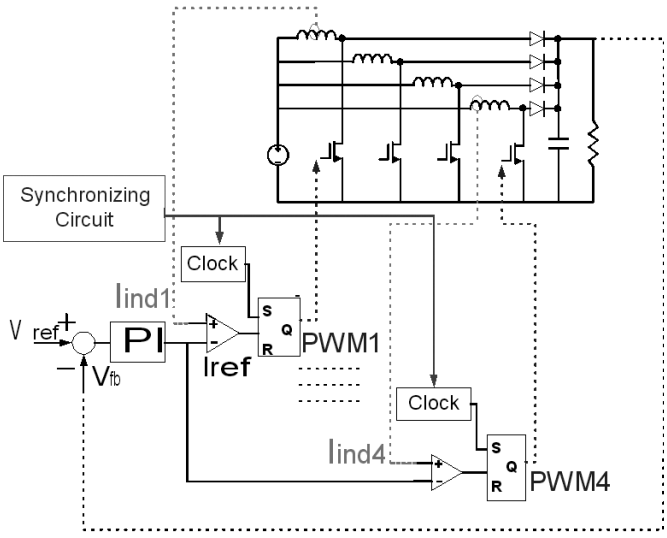

Fig. 5 : Analog Circuit Realization of the Polyphase Boost converter

Generation of the four phase shifted PWM signals can be done in two ways.

Method A: Programming general purpose timers with period of switching frequency and initializing four different counter regis-

Table II : Different Possibilities of On & Off Situations of Switches for N = 4

	Intervals	Switch	$0 \le D \le \frac{1}{4}$	$\frac{1}{4} \le D \le \frac{1}{2}$	$\frac{1}{2} \le D \le \frac{3}{4}$	$\frac{1}{2} \le D \le \frac{3}{4}$
1	$0 \le t \le \frac{Ts}{4}$	ON	1 0 0 0	1 0 0 1	1 0 1 1	1 1 1 1
2		OFF	0 0 0 0	1 0 0 0	1 0 0 1	1 0 1 1
3	$\frac{Ts}{4} \le t \le \frac{Ts}{2}$	ON	0 1 0 0	1 1 0 0	1 1 0 1	1 1 1 1
4		OFF	0 0 0 0	0 1 0 0	1 1 0 0	1 1 0 1
5	$\frac{Ts}{2} \le t \le \frac{3Ts}{4}$	ON	0 0 1 0	0 1 1 0	1 1 1 0	1 1 1 1
6		OFF	0 0 0 0	0 0 1 0	0 1 1 0	1 1 1 0
7	$\frac{3Ts}{4} \le t \le Ts$	ON	0 0 0 1	0 0 1 1	0 1 1 1	1 1 1 1
8		OFF	0 0 0 0	0 0 0 1	0 0 1 1	0 1 1 1

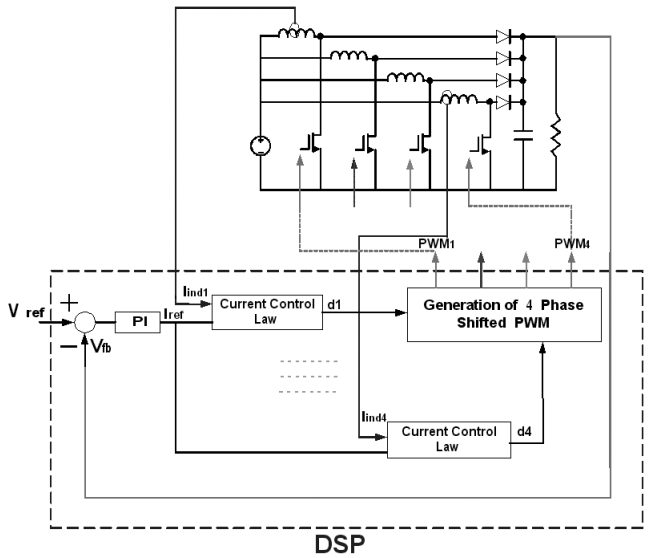

Fig. 6: Digital Circuit Realization of the Polyphase Boost converter

ters with 0, 90, 180, 270 degrees phase shift with respect to the timer period register.

Method B: The PWM signals can be generated on general-purpose input output pins. The switching pattern of different switches for different values of duty cycles, which is stored as lookup table in memory is shown in Table II. On time duration of the switch is determined by and similarly determines the off time duration.

Where D' is given by $D' = ND - \text{floor}(ND)$ (1)

Introducing the concept of D' is useful in analyzing the specifications of polyphase converter and in small signal averaging which has been previously achieved for the first time in [7].

Digital current control law

Like the original algorithm in [10], the required duty ratio for the present switching cycle is predicted based on the present current sample and the input and output voltages but not on the preceding duty ratio.

Fig. 7 shows the inductor current waveform. The sampled inductor current $i(n)$ at time nTs can be expressed as a function of the value of current $i(n-1)$ sampled in the previous switching period and the applied duty ratio $d(n)$.

$$i(n) = i(n-1) + \frac{v_{in} d[n] T_s}{L} + \frac{(v_{in} - v_o) d'[n] T_s}{L} \quad (2)$$

$$i(n) = i(n-1) + \frac{v_{in} T_s}{L} - \frac{(v_o) d'[n] T_s}{L} \quad (3)$$

By using $d' = 1 - d$ we can solve the above equation for predicting the duty cycle as given below

$$d[n] = \frac{L}{v_o T_s}(i_c - i[n-1]) + 1 - \frac{v_{in}}{v_o} \quad (4)$$

Where $i_c = i[n]$

In each switching cycle the inductor current follows the current reference i_c and tries to make the current error zero such that in steady state we have: $d[n] = 1 - v_{in}/v_o$

Equation (4) has a simpler form than equation (5) in [10] and has been derived based on a single cycle calculation.

As explained previously, sensing the currents were done in two ways. In the first method only one current is sampled and according to equation (4) the necessary duty cycle is obtained and loaded to all compare registers (for example, in method A which uses General Purpose Timers). This method is simple and produces good results, which is discussed later. In the second method all the currents are sampled such that each stage has an independent current control loop. Different duty ratio values, which are almost same, is found and loaded to corresponding compare registers. If minute differences are observed in the duty ratio values, which might cause difference in current sharing of parallel stages it can be rectified by adjusting the parameters in equation (4). Similarly by finding the average of different duty cycles, the error may be applied to force the current sharing.

Single sampling has the advantage of simplicity and consequently it is more suitable for higher switching frequency because only one current is sampled and is processed in lesser time. This method is good if the component values (for example the inductor values in different stages) are almost equal such that no significance difference in current sharing is observed. On the other hand multiple sampling has the property to adjust each duty ratio value independently despite changes in component values in other stages. Applying the average of the duty ratio values is another option to improve the performance in closed loop control of these converters. However it should be noted that this method takes more time compared with single sampling method.

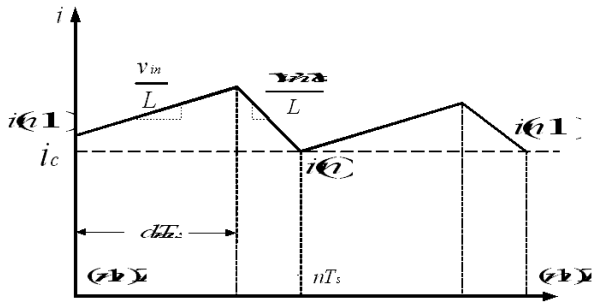

Fig. 7: Inductor Current Waveform under Valley Current Control

It is essential to note that some techniques, which have been explained here, like adjusting the parameters in each control loop and applying the average duty value can only be achieved in digital control implementation. Another technique, which does not exist in analog implementation, is turning off of some of the converters at light load operation during which converters move into Discontinuous Mode of Operation. According to the level of load current, one, two or three of the converters may be switched off and in each case generation of the phase shifted PWM may change. For example for four converters in parallel one can turn off two or three of the stages without changing the generation of phase shifted PWM signals. Of course for turning off of one stage or any other numbers in general in N converters in parallel the required amount of phase shift varies and it can be predetermined and stored in memory.

Comparing specifications

Inductor size

By comparing two converters at the same condition i.e. same output power, same output voltage and same amount of ripple current in the inductors it is easy to show that for single stage

$$I_L = \frac{I_{load}}{1-D} \tag{5}$$

And for N converters in parallel

$$I_L = \frac{I_{load}}{N(1-D)} \tag{6}$$

Hence for same value of $\Delta I_L/I_L$ it is required that $L_n = NL$ (7)

As the product of A_cA_w remains same value in both single stage and N-parallel connected boost converters it means in practice the total size of N inductors are almost equal to the size of single stage inductor.

RHP Zero

From the dynamical equation one can derive output to control transfer function. The results show that the RHP Zero does not change because in the single stage the RHP Zero equals to

V_g/L_{IL} (8)

And for N converters in parallel it equals to

$$\frac{V_g}{(NL)(\frac{I_L}{N})} \tag{9}$$

From the dynamical equation and with the aid of matrices in relations (6), (7) the equality of the above result can be numerically justified.

Output resistance

Again from the dynamical equation the output impedance or in case of output DC current the output resistance of the N parallel converter comes down substantially so that for $N = 4$, $L_1 = L_2 = L_3 = L_4 = 50$ µH, $C = 1000$ µF, $R_c = 0.02$, $V_o = 32$ and $D = 0.5$.

$$\frac{R_{O4}}{R_{O1}} = 0.1244$$

The curve for the different values of D has been sketched in Fig. 8 Where $R_{based} = R_{o1}$ (Output resistance of single stage)

RMS Current of Capacitor

One of the interesting point is the RMS current of the output capacitor. Fig. 9 shows the waveform of the current of output capacitor. $I_{load} = 10$, $\Delta_{IL} = 20$ %, $D = 0.7$

With a good approximation the RMS current of the output Capacitor can be expressed by

$$I_{rms} = I_L\sqrt{(ND-K+1)(K-ND)} \tag{10}$$

Where $K = \text{floor}(ND)+1$ & $I_L = \frac{I_{load}}{N(1-D)}$ and "floor" shows the integer part function

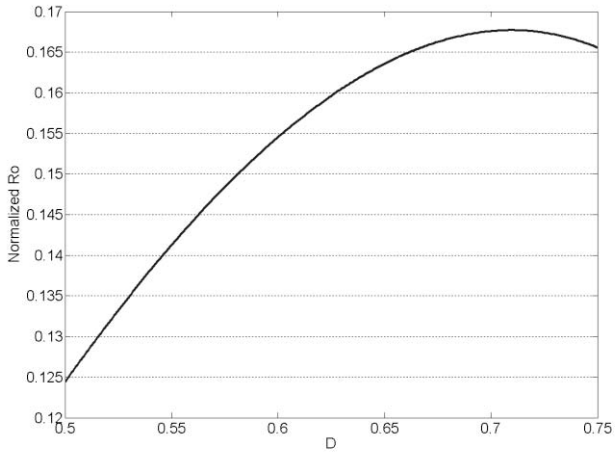

Fig. 8: The Normalized Output Resistance ($N = 4$)

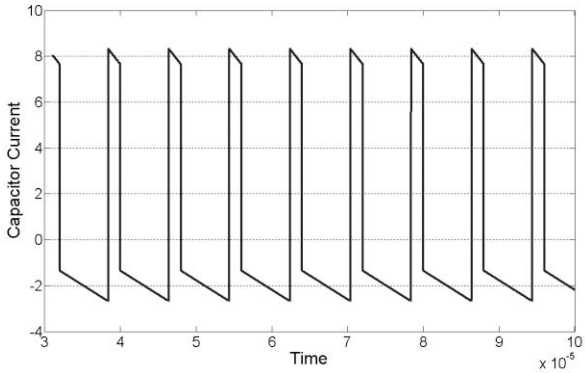

Fig. 9 : The Current of the Output Capacitor ($D = 0.7$)

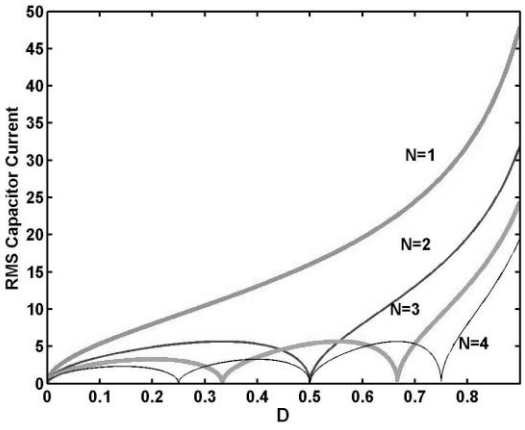

Fig. 10: The RMS Capacitor Current for different *N*

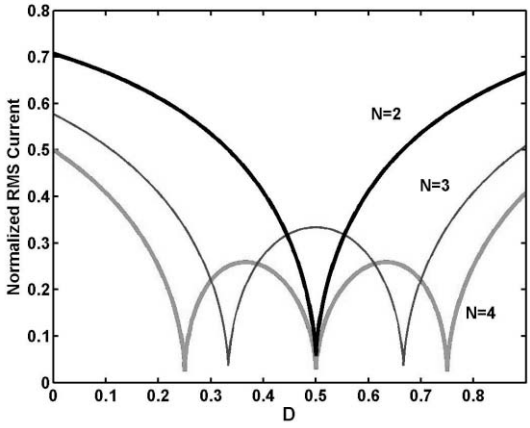

Fig. 11: The Normalized RMS Capacitor Current

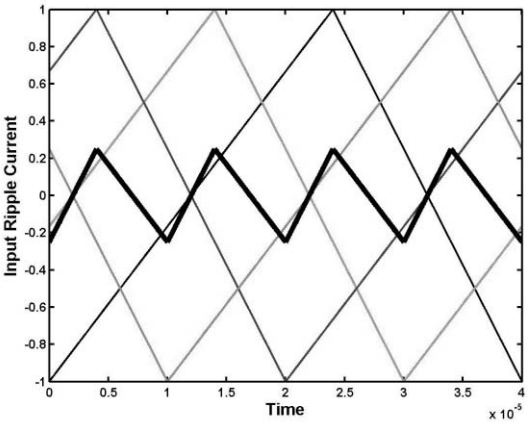

Fig. 12: Input ripple Current for N = 4 & D = 0.6

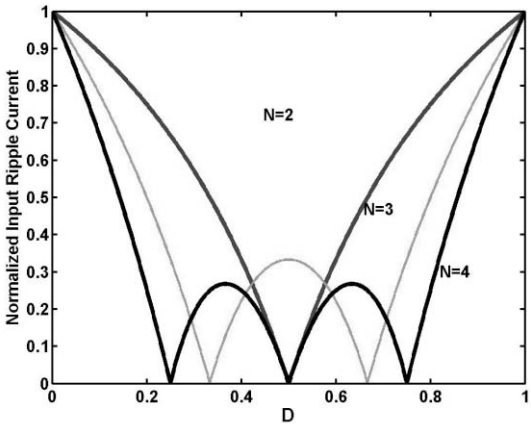

Fig.13: Normalized Input Ripple Current

Or equivalently it can be written as $I_{rms} = I_L \sqrt{D'(1-D')}$ (11)

Where $D' = ND - floor(ND)$

For I_{load} = 16, V_g = 8. Fig. 10 shows the RMS current for different values of N. In Fig. 10 the converters are under similar conditions i.e. same output power; same output voltage and same amount of ripple current in the inductors. Fig. 11 shows the normalized RMS capacitor current where the RMS base current is the capacitor current in a single stage. It may be seen that the capacitor ripple current fall at least by a factor of N, but can be even smaller for certain duty ratios, such as 0.25, 0.5, 0.75, etc.

Input ripple current

The input current is at higher frequency than the switching frequency and hence the EMI filter will be lighter and as it can be seen from Fig. 12 the peak to peak-input ripple current is substantially reduced and the magnitude of this current ripple for polyphase boost converter can be derived as [6].

$$\Delta I_{in,N} = \frac{(K-ND)(ND-k+1)}{ND(1-D)} \Delta I_{in,1} \quad (12)$$

Where, $K = 1, 2, ..., N, \frac{K-1}{N} \le D \le \frac{K}{N}$

Or equivalently

$$\Delta I_{in,N} = \frac{D'(1-D')}{ND(1-D)} \Delta I_{in,1} \quad (13)$$

And $\Delta I_{in,1} = \frac{Vg}{L} DTs$ (14)

The normalized magnitude of this ripple as a function of D and for different values of N has been sketched in Fig. 13. Again the improvement is at least by a factor of N.

Output ripple voltage

Based on the previous analysis and the relation for output ripple voltage

That is

$$\frac{\Delta Vo}{Vo} = \frac{DTs}{R_{load} C} \quad (15)$$

The output ripple voltage for N converters is given by

$$\left(\frac{\Delta Vo}{Vo}\right)_N = \frac{D'(1-D')}{N^2 D(1-D)} \left(\frac{\Delta Vo}{Vo}\right)_1 \quad (16)$$

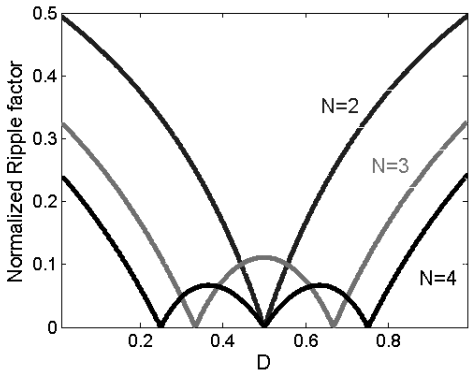

Fig. 14 : Normalized Ripple Factor of Output Voltage

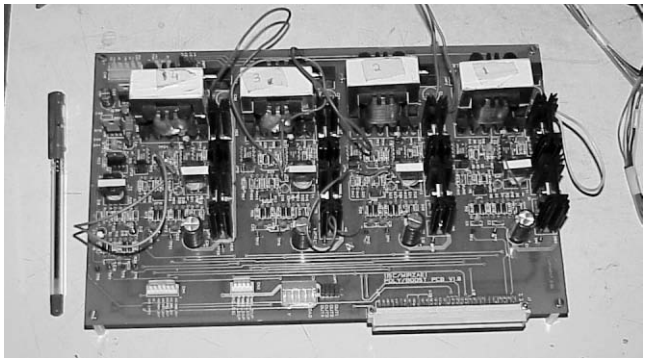

Fig. 15: Prototype Board with Four Boost Converters in Parallel

For the same amount of ripple in the output the size of capacitor reduces by a factor, which is equal to

$$\frac{D'(1-D')}{N^2 D(1-D)}$$

and it has been sketched for different values of N and D in Fig. 14

Circuit realization

A prototype with four boost converters in parallel has been implemented. Each boost converter has a specification of 35 W and each is operating under 90-degree phase shift in control circuit. Its input voltage is 12 V and output voltage is 32 V. The inductor current ripple is 20 % of its average value. The switch currents are sensed through current transformers and they go to the ADC part of DSP control board. The circuit uses an edge-blanking feature to ignore the reverse recovery current of diode. Gate driver circuit is optically isolated from the DSP board and the output feedback is taken from an isolated transformer. The MOSFET IRF244 and diode BYQ 28E-200 are used in the circuit. The switching frequency is 200 kHz. The controller is a TI's general-purpose starter kit eZdspF2812. It has a 150 MHz clock with 12-bit ADC, which is working at maximum 25 MHz clock speed. The code has been written in assembly language.

Fig. 15 shows the prototype circuit. The board has bigger size than its actual size because at first it was designed to work at 25 kHz switching frequency so the inductors are bulky. In addition to that we designed the board appropriately to be interfaced with either a DSP controller or a FPGA controller.

Experimental results

The waveform in Fig. 16 show Phase shifted PWM waveforms along with one of the inductors current switched at 200 kHz. Fig. 17 shows the situation which two of these converters are working in parallel and the other two converters are off. The output capacitor current has been measured under the same output power for N = 4 and N = 1 and as it can be seen from Figs. 18 and 19 there is meaningful difference between them. Figs. 20 shows the current sharing of parallel converters when only one of the currents is sampled and the numbers 2.2A and 2.1A corresponds to Ch1and Ch4 in Fig. 20 verifies that the current sharing are almost equal. Similar results for the level of currents of the other two converters (Ch1 and Ch4) are observed in Fig. 21. The improvement in input ripple current as we expected is seen in Fig. 22.

Conclusion

This paper discusses digital control method for polyphase boost converter. A modified method for determining the duty cycle corresponds to current control has been developed. The size of N boost converters in parallel is almost same as a single boost converter of the same total power because the size of main parts-inductors-almost remains same.

Both simulations and measurements show polyphase boost converter has several advantages over single boost converter Smaller RMS current in the energy-storage capacitor, lower input ripple current and lower output ripple voltage or smaller size of the tank capacitor are those important points, which have been considered. As it can be seen from Figs. 18 and 19 the peak current of output capacitor for N = 4 and N = 1 are 0.688 A and 3.50 A respectively and the ratio is equal to 0.197 which matches with simulation

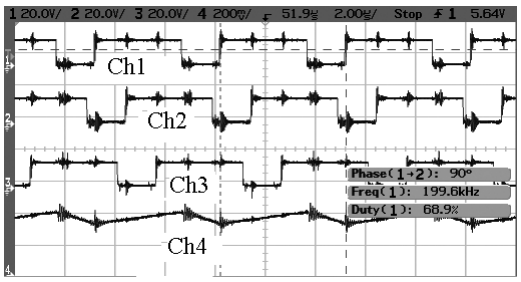

Fig. 16: Phase Shifted PWM Waveforms
Ch1, Ch2, Ch3: Gate Drive Voltages 20 V/div
Ch4: Inductor Current 0.2 A/div
Horizontal Scale: 2 µs/div, f = 200 kHz

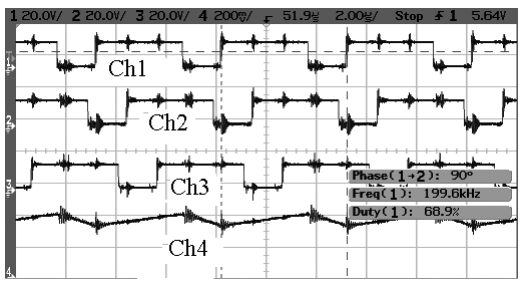

Fig. 17: Two Converters are working
Ch1, Ch2: Gate Drive Voltages 20 V/div
Ch3, Ch4: Inductor Currents 0.2 A/div
Horizontal Scale: 2 µs/div, f = 200 kHz

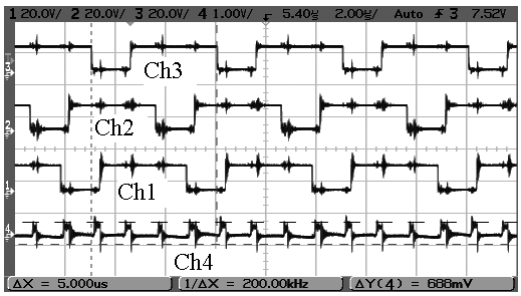

Fig. 18: Output Capacitor Current for $N = 4$
Ch1, Ch2 , Ch3: Gate Drive Voltages 20 V/div
Ch4: Output Capacitor Current 1 A/div
Horizontal Scale: 2 µs/div, $f = 200$ kHz

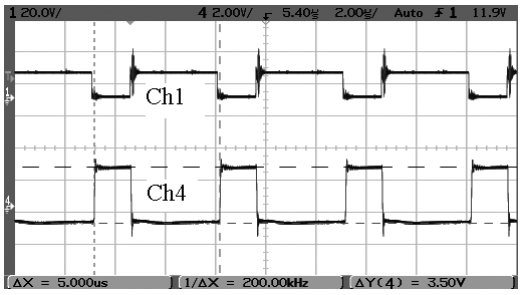

Fig. 19: Output Capacitor Current for $N = 1$
Ch1: Gate Drive Voltage 20 V/div
Ch4: Output Capacitor Current 2 A/div
Horizontal Scale: 2 µs/div, $f = 200$ kHz

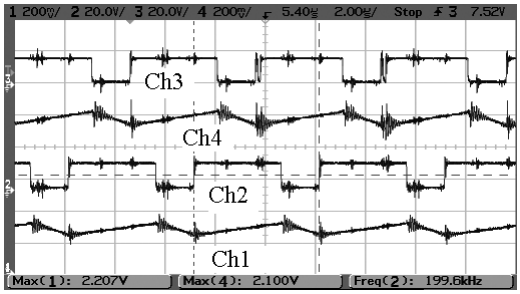

Fig. 20: Current Sharing of 2 Converters in Parallel
Ch2, Ch3: Gate Drive Voltages 20 V/div
Ch1, Ch4: Inductor Currents 0.2 A/div
Horizontal Scale: 2 µs/div, $f = 200$ kHz

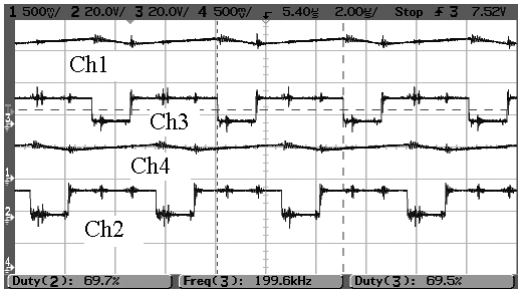

Fig. 21: Current Sharing of Other 2 Stages
Ch2, Ch3: Gate Drive Voltages 20 V/div
Ch1, Ch4: Inductor Currents 0.5 A/div
Horizontal Scale: 2 µs/div, $f = 200$ kHz

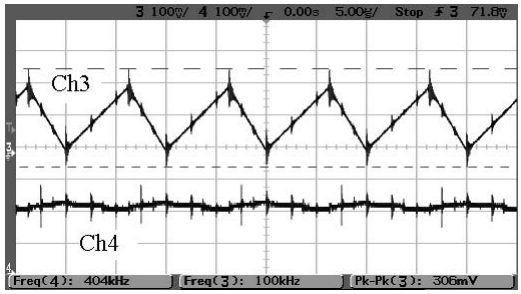

Fig. 22: Input Ripple Current for $N = 4$
Ch3: Input Ripple Current 0.1 A/div
Ch4: Inductor Ripple Current 0.1 A/div
Horizontal Scale: 5 µs/div, $f = 100$ kHz

results from Fig. 11 and similarly the ratio of input ripple current for $N = 4$ and $N = 1$ is less than 40 mA/200 mA = 0.2 which is almost matches with simulation results of Fig 13.

Digital realization in control results in better performance and advantages, which cannot be achieved by analog method. Programmability, modularity and flexibility in design and different operating conditions are major points, which have been addressed.

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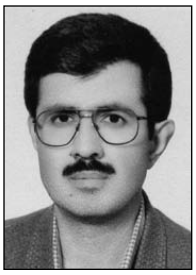

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